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L1 and (multi adj1 thread$2)	34

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L1	decod$3 same packet same process$3 same memory	2176	L1

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	L1 and (multi adj1 thread$2)	34	L2
L1	decod$3 same packet same process$3 same memory	2176	L1

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Terms	Documents
(370/912 |709/102 |710/100 |710/3 |710/52 |710/56 |710/74 |710/5 |711/161 |711/100 |711/5 |711/154 |712/205 |712/208 |712/221).ccls.	8957

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Search: L4

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	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L3	L2	0	L3
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L2	L1 and (multi adj1 thread$2)	34	L2
L1	decod$3 same packet same process$3 same memory	2176	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L2 and L4	3

Database:
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EPO Abstracts Database
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Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search | Recall Text | Clear | Interrupt

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Set Name side by side	Query	Hit Count	Set Name result set
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L4	710/100,3,52,56,74,5;712/205,208,221;709/102;711/161,100,5,154;370/912.ccls.	8957	L4
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L3	L2	0	L3
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L2	L1 and (multi adj1 thread$2)	34	L2
L1	decod$3 same packet same process$3 same memory	2176	L1

END OF SEARCH HISTORY

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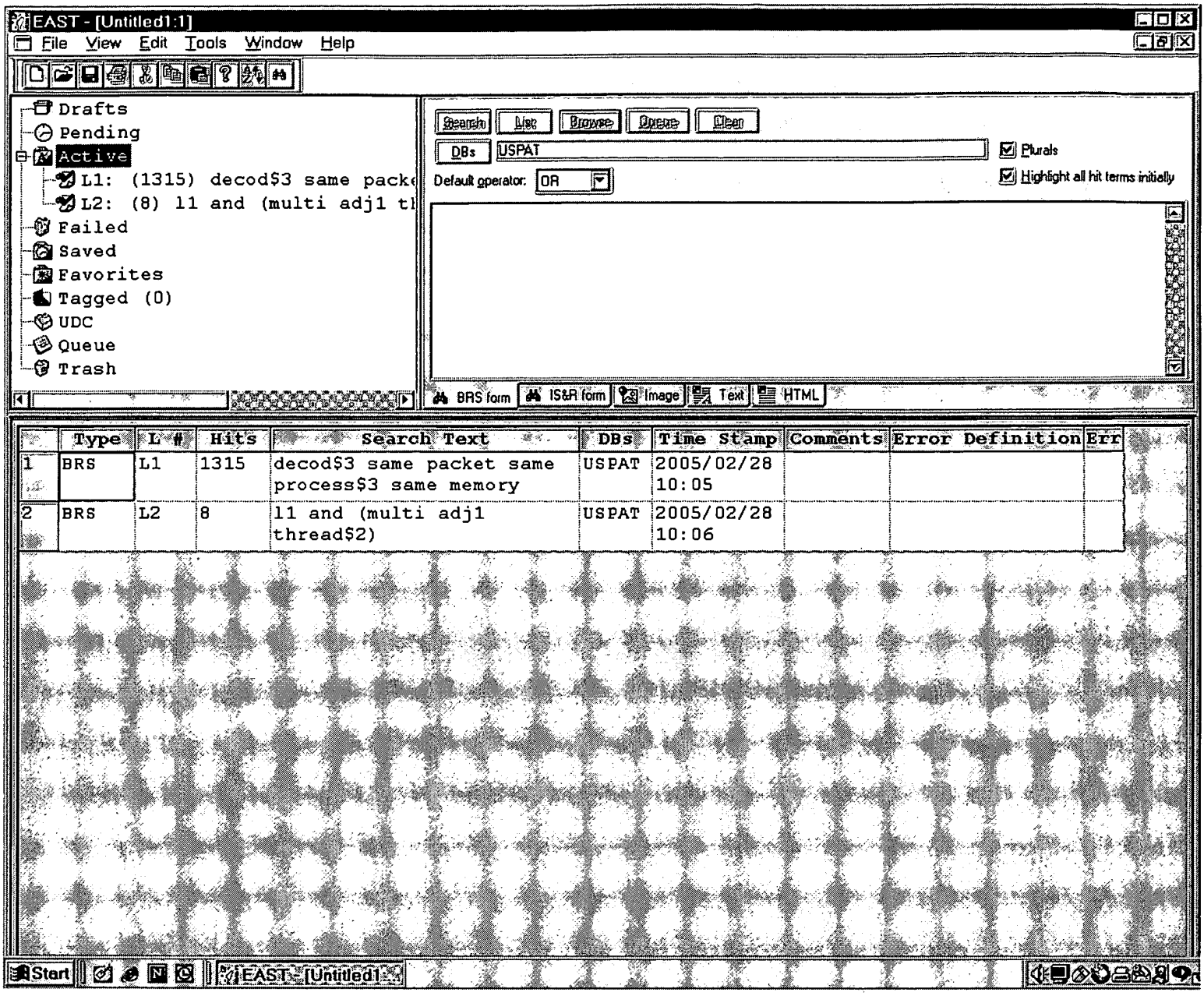
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2 BRS L2 8 l1 and (multi adj1 thread$2) USPAT 2005/02/28 10:06
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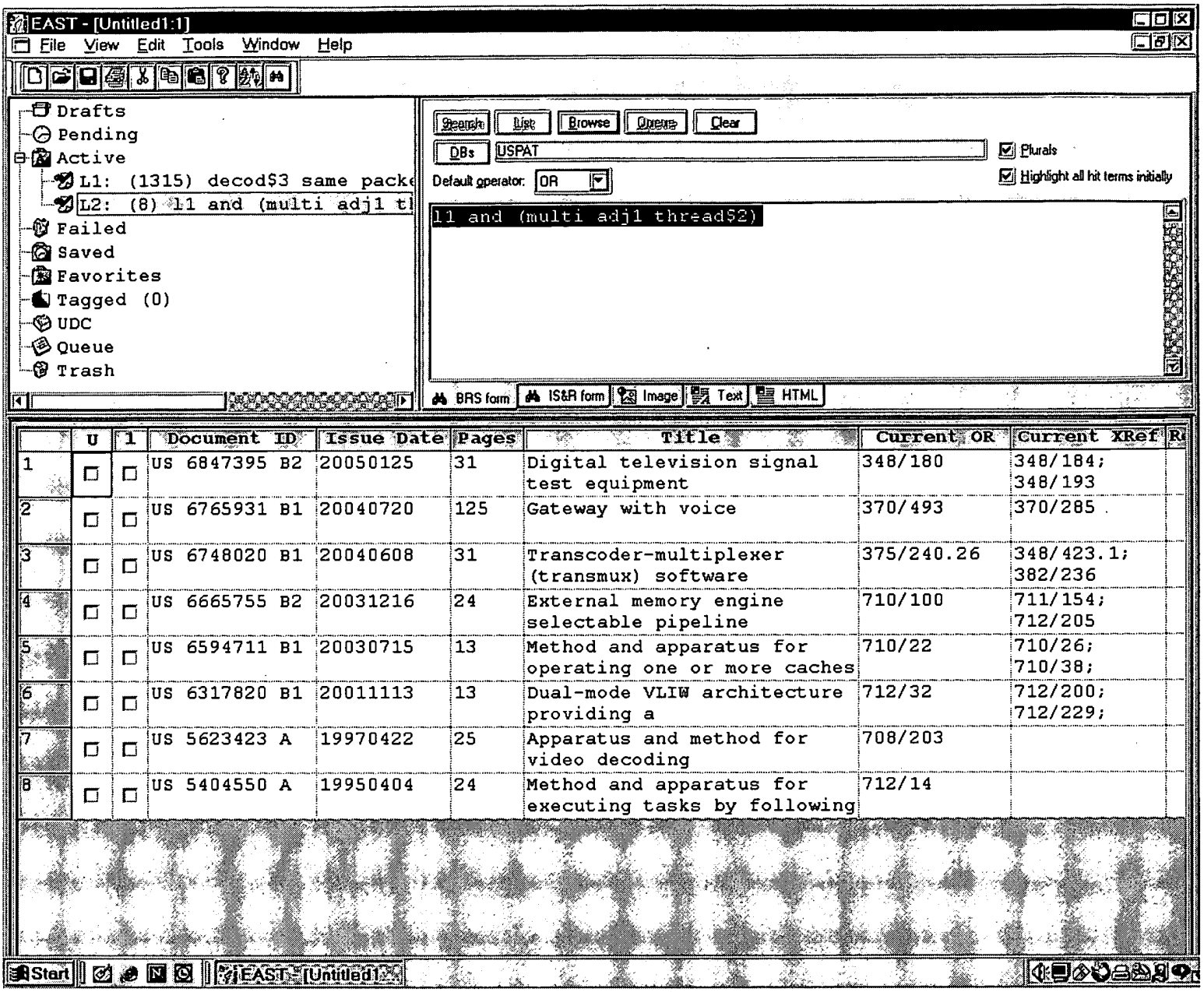

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 6847395 B2	20050125	31	Digital television signal test equipment	348/180	348/184; 348/193	
2	☐	☐	US 6765931 B1	20040720	125	Gateway with voice	370/493	370/285	
3	☐	☐	US 6748020 B1	20040608	31	Transcoder-multiplexer (transmux) software	375/240.26	348/423.1; 382/236	
4	☐	☐	US 6665755 B2	20031216	24	External memory engine selectable pipeline	710/100	711/154; 712/205	
5	☐	☐	US 6594711 B1	20030715	13	Method and apparatus for operating one or more caches	710/22	710/26; 710/38;	
6	☐	☐	US 6317820 B1	20011113	13	Dual-mode VLIW architecture providing a	712/32	712/200; 712/229;	
7	☐	☐	US 5623423 A	19970422	25	Apparatus and method for video decoding	708/203		
8	☐	☐	US 5404550 A	19950404	24	Method and apparatus for executing tasks by following	712/14		

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---

1 **Design and component test of SFQ shift register memories**
Fujiwara, K.; Hoshina, H.; Yamashiro, Y.; Yoshikawa, N.;
Applied Superconductivity, IEEE Transactions on , Volume: 13 , Issue: 2 , Jun 2003
Pages:555 - 558

[Abstract] [PDF Full-Text (485 KB)] **IEEE JNL**

---

2 **Long-term memory motion-compensated prediction for robust video transmission**
Wiegand, T.; Farber, N.; Stuhlmuller, K.; Girod, B.;
Image Processing, 2000. Proceedings. 2000 International Conference on , Vol 2 , 10-13 Sept. 2000
Pages:152 - 155 vol.2

[Abstract] [PDF Full-Text (416 KB)] **IEEE CNF**

---

3 **Packet loss protection of embedded data with fast local search**
Stankovic, V.; Hamzaoui, R.; Zixiang Xiong;
Image Processing. 2002. Proceedings. 2002 International Conference on , Vol 2 , 22-25 Sept. 2002
Pages:II-165 - II-168 vol.2

[Abstract] [PDF Full-Text (431 KB)] **IEEE CNF**

---

4 **Reconstruction of missing packets for CELP-based speech coders**
Husain, A.; Cuperman, V.;
Acoustics, Speech, and Signal Processing, 1995. ICASSP-95., 1995 Internatio Conference on , Volume: 1 , 9-12 May 1995
Pages:245 - 248 vol.1

h eee e eee g e ch e ch e e c e e ec e

[Abstract] [PDF Full-Text (364 KB)] IEEE CNF

5 **A single chip teletext decoder including data slicer**
Lyne, C.R.W.;
Consumer Electronics, 1989. Digest of Technical Papers. ICCE., IEEE 1989 International Conference on , 6-9 June 1989
Pages:164 - 165

[Abstract] [PDF Full-Text (148 KB)] IEEE CNF

6 **Adaptive Viterbi Algorithm With ARQ for Bounded Complexity Decod**
Harvey, B.A.;
Wireless Communications, IEEE Transactions on , Volume: 3 , Issue: 6 , Nov.

Pages:1948 - 1952

[Abstract] [PDF Full-Text (232 KB)] IEEE JNL

7 **Implementation of a video transcoder for embedded system**
Lehtoranta, O.; Kukkala, P.; Hamalainen, T.D.; Lappalainen, V.;
Information Technology: Coding and Computing [Computers and Communicat 2003. Proceedings. ITCC 2003. International Conference on , 28-30 April 200
Pages:389 - 395

[Abstract] [PDF Full-Text (325 KB)] IEEE CNF

8 **A packet loss concealment algorithm based on time-scale modificati for CELP-type speech coders**
Moon-Keun Lee; Sung-Kyo Jung; Hong-Goo Kang; Young-Cheol Park; Dae-He Youn;
Acoustics, Speech, and Signal Processing, 2003. Proceedings. (ICASSP '03). 2 IEEE International Conference on , Volume: 1 , 6-10 April 2003
Pages:I-116 - I-119 vol.1

[Abstract] [PDF Full-Text (354 KB)] IEEE CNF

9 **Low-memory packetized SPIHT image compression**
Wheeler, F.W.; Pearlman, W.A.;
Signals, Systems, and Computers, 1999. Conference Record of the Thirty-Thir Asilomar Conference on , Volume: 2 , 24-27 Oct. 1999
Pages:1193 - 1197 vol.2

[Abstract] [PDF Full-Text (568 KB)] IEEE CNF

10 **Few decoders in the encoder: a low complexity encoding strategy f H.26L**
Olmo, G.; Cucco, C.; Grangetto, M.; Magli, E.;
Acoustics, Speech, and Signal Processing, 2003. Proceedings. (ICASSP '03). 2 IEEE International Conference on , Volume: 3 , 6-10 April 2003
Pages:III - 641-4 vol.3

[Abstract] [PDF Full-Text (384 KB)] IEEE CNF

11 **Transmission of MPEG-2 video streams over ATM**
Lewis, A.; Gringeri, S.; Khasnabish, B.; Basch, B.;
MILCOM 97 Proceedings , Volume: 1 , 2-5 Nov. 1997
Pages:237 - 241 vol.1

[Abstract] [PDF Full-Text (588 KB)] **IEEE CNF**

---

12 **An efficient high-speed block turbo code decoding algorithm and hardware architecture design**
Kyungchul Yoo; Hyungshik Shin; Yunho Jung; Junghyuck Lee; Jaeseok Kim;
Signal Processing Systems, 2003. SIPS 2003. IEEE Workshop on , 27-29 Aug.

Pages:41 - 44

[Abstract] [PDF Full-Text (318 KB)] **IEEE CNF**

---

13 **The impacts of errors and delays on the performance of MPEG2 vid communications**
Mehaoua, A.; Boutaba, R.;
Acoustics, Speech, and Signal Processing, 1999. ICASSP '99. Proceedings., 19
IEEE International Conference on , Volume: 4 , 15-19 March 1999
Pages:2195 - 2198 vol.4

[Abstract] [PDF Full-Text (300 KB)] **IEEE CNF**

---

14 **Low-power bit-serial Viterbi decoder for next generation wide-ban CDMA systems**
Suzuki, H.; Yun-Nan Chang; Parhi, K.K.;
Acoustics, Speech, and Signal Processing, 1999. ICASSP '99. Proceedings., 19
IEEE International Conference on , Volume: 4 , 15-19 March 1999
Pages:1913 - 1916 vol.4

[Abstract] [PDF Full-Text (368 KB)] **IEEE CNF**

---

15 **Pattern matching and parallel processing with CCD technology**
Pedroni, V.A.; Agranat, A.; Neugebauer, C.; Yariv, A.;
Neural Networks, 1992. IJCNN., International Joint Conference on , Volume: 3
11 June 1992
Pages:620 - 623 vol.3

[Abstract] [PDF Full-Text (212 KB)] **IEEE CNF**

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An efficient high-speed block turbo code decoding algorithm and hardware architecture design

Kyungchul Yoo Hyungshik Shin Yunho Jung Junghyuck Lee Jaeseok Kim
Yonsei Univ., Seoul, South Korea

This paper appears in: **Signal Processing Systems, 2003. SIPS 2003. IEE Workshop on**

Publication Date: 27-29 Aug. 2003
On page(s): 41 - 44
ISSN: 1520-6130
Number of Pages: xii+395
Inspec Accession Number: 7854623

Abstract:
We propose a high speed block turbo code **decoding** algorithm and design ha architecture. Block turbo codes (BTCs) support variable code rates and **packe** show a high-performance owing to a soft decision iterative **decoding** of turbc However, BTCs have a long **decoding** time because of an iterative **decoding** complicated extrinsic information operation. The proposed algorithm, using th that represents channel information, reduces the long **decoding** time. The th decided by the absolute mean and the standard deviation of an LLR (log likeli in consideration that the LLR distribution is Gaussian. As a result of logic synt 0.35 /spl mu/m CMOS technology, it is proved that the **decoder** applied by tl algorithm reduces the **decoding** time by about 30% and includes about 20K and 32 Kbit **memory** size.

Index Terms:
CMOS logic circuits Gaussian distribution block codes integrated circuit design itera **decoding** logic design turbo codes variable rate codes 0.35 micron 32 Kbit CMC technology Gaussian distribution block turbo codes channel information hardware a design high-speed **decoding** algorithm log likelihood ratio logic synthesis multimed communication soft decision iterative **decoding** standard deviation variable code rat **packet** sizes

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☐ 1. Document ID: US 20020116587 A1

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L5: Entry 1 of 3 File: PGPB Aug 22, 2002

PGPUB-DOCUMENT-NUMBER: 20020116587
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020116587 A1

TITLE: External memory engine selectable pipeline architecture

PUBLICATION-DATE: August 22, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Modelski, Richard P.	Hollis	NH	US	
Craren, Michael J.	Holliston	MA	US	
Kristiansen, Adrian M.	Somerville	MA	US	

US-CL-CURRENT: 711/154

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6665755 B2

L5: Entry 2 of 3 File: USPT Dec 16, 2003

US-PAT-NO: 6665755
DOCUMENT-IDENTIFIER: US 6665755 B2

TITLE: External memory engine selectable pipeline architecture

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6594711 B1

L5: Entry 3 of 3 File: USPT Jul 15, 2003

US-PAT-NO: 6594711
DOCUMENT-IDENTIFIER: US 6594711 B1

TITLE: Method and apparatus for operating one or more caches in conjunction with

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direct memory access controller

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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PGPUB-DOCUMENT-NUMBER: 20020116587
PGPUB-FILING-TYPE: new
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TITLE: External memory engine selectable pipeline architecture

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NAME	CITY	STATE	COUNTRY	RULE-47
Modelski, Richard P.	Hollis	NH	US	
Craren, Michael J.	Holliston	MA	US	
Kristiansen, Adrian M.	Somerville	MA	US	

APPL-NO: 09/ 742286 [PALM]
DATE FILED: December 22, 2000

INT-CL: [07] G06 F 13/00

US-CL-PUBLISHED: 711/154
US-CL-CURRENT: 711/154

REPRESENTATIVE-FIGURES: 1A

ABSTRACT:

External memory engine selectable pipeline architecture provides external memory to a multi-thread packet processor which processes data packets using a multi-threaded pipelined machine wherein no instruction depends on a preceding instruction because each instruction in the pipeline is executed for a different thread. The route switch packet architecture transfers a data packet from a flexible data input buffer to a packet task manager, dispatches the data packet from the packet task manager to a multi-threaded pipelined analysis machine, classifies the data packet in the analysis machine, modifies and forwards the data packet in a packet manipulator. The route switch packet architecture includes an analysis machine having multiple pipelines, wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field, a packet task manager, a packet manipulator, a global access bus including a master request bus and a slave request bus separated from each other and pipelined, an external memory engine, and a hash engine.

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US006748020B1

(12) **United States Patent**
Eifrig et al.

(10) Patent No.: **US 6,748,020 B1**
(45) Date of Patent: **Jun. 8, 2004**

(54) **TRANSCODER-MULTIPLEXER (TRANSMUX) SOFTWARE ARCHITECTURE**

(75) Inventors: **Robert O. Eifrig**, San Diego, CA (US); **Fan Ling**, Santa Clara, CA (US); **Xuemin Chen**, San Diego, CA (US)

(73) Assignee: **General Instrument Corporation**, Horsham, PA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 736 days.

(21) Appl. No.: **09/696,533**

(22) Filed: **Oct. 25, 2000**

(51) Int. Cl.[7] **H04N 7/12**; G06K 9/36
(52) U.S. Cl. 375/240.26; 382/236; 348/423.1
(58) Field of Search 375/240.25, 240.23, 375/240.29, 240.03, 240.12, 240.04, 240.01; 348/458, 459, 365.1, 405.1, 423.1; 370/535, 473; 382/234, 235

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,805,224	A *	9/1998	Kassman et al.	375/240.04
5,870,146	A	2/1999	Zhu	
6,094,457	A	7/2000	Linzer et al.	
6,275,236	B1 *	8/2001	Chen et al.	375/240.25
6,310,915	B1 *	10/2001	Wells et al.	375/240.03
6,434,197	B1 *	8/2002	Wang et al.	375/240.29
6,570,922	B1 *	1/2003	Wang et al.	375/240.12
6,643,327	B1 *	11/2003	Wang	375/240.12

FOREIGN PATENT DOCUMENTS

EP	0 572 766	12/1993
EP	1 001 382	5/2000
WO	WO 97/09584	10/1997
WO	WO 97/40625	10/1997
WO	WO 98/27720	6/1998
WO	WO 00/07374	2/2000

OTHER PUBLICATIONS

Media Accelerated Processor for Consumer Appliances, MAPCA2100™ Data Sheet, DS400006 Feb. 5, 2000, Equator Technologies, Inc.

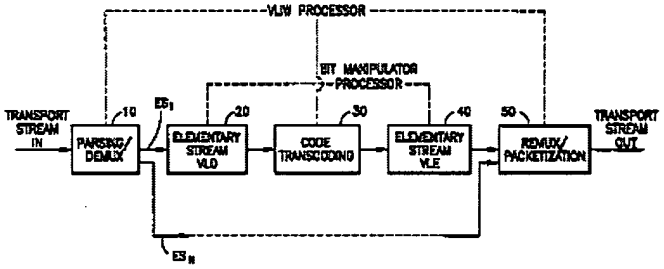
* cited by examiner

Primary Examiner—Gims Philippe
(74) *Attorney, Agent, or Firm*—Barry R. Lipsitz; Douglas M. McAllister

(57) **ABSTRACT**

A digital video transcoder-multiplexer (transmux) architecture that is fully software-implemented. The transmux includes transcoder processing elements (TPEs) that may use a very long instruction word (VLIW) media processor for performing transcoding, and de-assembly and re-assembly at a transport stream level, and a co-processor for providing de-assembly and re-assembly at an elementary stream level. The processors operate in parallel, at least in part, to optimize throughput and provide processing load balancing. A transmux architecture that is fully software implemented is provided to allow upgrading to handle new functions, fix hardware or software problems, test new processes, adapt to changing customer requirements, and so forth.

27 Claims, 14 Drawing Sheets



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(12) **United States Patent**
Eifrig et al.

(10) **Patent No.: US 6,748,020 B1**
(45) **Date of Patent: Jun. 8, 2004**

(54) **TRANSCODER-MULTIPLEXER (TRANSMUX) SOFTWARE ARCHITECTURE**

(75) Inventors: **Robert O. Eifrig**, San Diego, CA (US); **Fan Ling**, Santa Clara, CA (US); **Xuemin Chen**, San Diego, CA (US)

(73) Assignee: **General Instrument Corporation**, Horsham, PA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 736 days.

(21) Appl. No.: **09/696,533**

(22) Filed: **Oct. 25, 2000**

(51) Int. Cl.[7] H04N 7/12; G06K 9/36

(52) U.S. Cl. 375/240.26; 382/236; 348/423.1

(58) Field of Search 375/240.26, 240.25, 375/240.29, 240.03, 240.12, 240.04, 240.01; 348/458, 459, 365.1, 405.1, 423.1; 370/535, 473; 382/234, 235

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,805,224	A *	9/1998	Kesman et al.	375/240.04
5,870,146	A	2/1999	Zhu	
6,094,457	A	7/2000	Linzer et al.	
6,275,536	B1 *	8/2001	Chen et al.	375/240.25
6,310,915	B1 *	10/2001	Wells et al.	375/240.03
6,434,197	B1 *	8/2002	Wang et al.	375/240.29
6,570,922	B1 *	1/2003	Wang et al.	375/240.12
6,643,327	B1 *	11/2003	Wang	375/240.12

FOREIGN PATENT DOCUMENTS

EP	0 573 765	12/1993
EP	1 001 582	5/2000
WO	WO 97/39584	10/1997
WO	WO 97/40625	10/1997
WO	WO 98/27720	6/1998
WO	WO 00/07374	2/2000

OTHER PUBLICATIONS

Media Accelerated Processor for Consumer Appliances, MAPCA2000™ Data Sheet, DS4000006 Feb. 5, 2000, Equator Technologies, Inc.

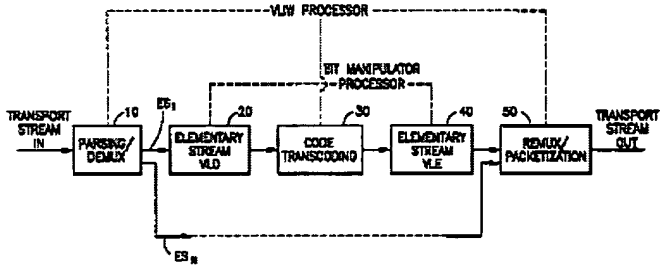
* cited by examiner

Primary Examiner—Cicus Philippe
(74) *Attorney, Agent, or Firm*—Barry R. Lipsitz; Douglas M. McAllister

(57) **ABSTRACT**

A digital video transcoder-multiplexer (transmux) architecture that is fully software-implemented. The transmux includes transcoder processing elements (TPEs) that may use a very long instruction word (VLIW) media processor for performing transcoding, and de-assembly and re-assembly at a transport stream level, and a co-processor for providing de-assembly and re-assembly at an elementary stream level. The processors operate in parallel, at least in part, to optimize throughput and provide processing load balancing. A transmux architecture that is fully software implemented is provided to allow upgrading to handle new functions, fix hardware or software problems, test new processes, adapt to changing customer requirements, and so forth.

27 Claims, 14 Drawing Sheets



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US006665755B2

(12) **United States Patent**
Modelski et al.

(10) **Patent No.: US 6,665,755 B2**
(45) **Date of Patent: Dec. 16, 2003**

(54) **EXTERNAL MEMORY ENGINE SELECTABLE PIPELINE ARCHITECTURE**

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(73) Assignee: **Nortel Networks Limited** (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 456 days.

(21) Appl. No.: **09/742,286**

(22) Filed: **Dec. 22, 2000**

(65) **Prior Publication Data**

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(51) Int. Cl.[7] G06F 13/00; G06F 12/00
(52) U.S. Cl. 710/100; 711/154; 712/205
(58) Field of Search 710/100, 3, 52, 710/56, 74, 5; 712/203, 208, 221; 709/102; 711/151, 100, 5, 154; 370/912

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,112,489 A * 9/1978 Wood
5,255,211 A * 10/1993 Redmond
5,619,723 A * 4/1997 Jones et al.

* cited by examiner

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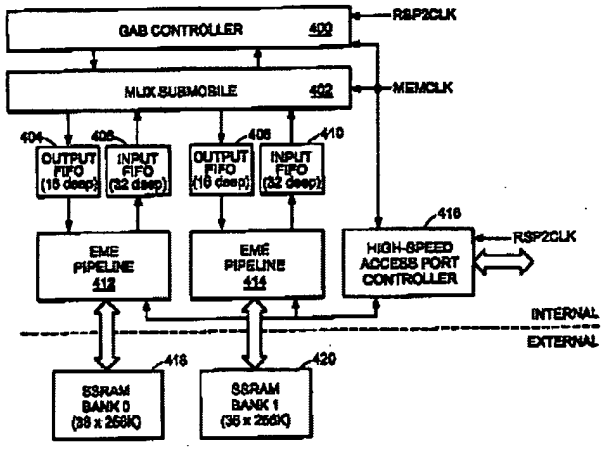
(57) **ABSTRACT**

External memory engine selectable pipeline architecture provides external memory to a multi-thread packet processor which processes data packets using a multi-threaded pipelined machine wherein no instruction depends on a preceding instruction because each instruction in the pipeline is executed for a different thread. The route switch packet architecture transfers a data packet from a flexible data input buffer to a packet task manager, dispatches the data packet from the packet task manager to a multi-threaded pipelined analysis machine, classifies the data packet in the analysis machine, modifies and forwards the data packet in a packet manipulator. The route switch packet architecture includes an analysis machine having multiple pipelines, wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field, a packet task manager, a packet manipulator, a global access bus including a master request bus and a slave request bus separated from each other and pipelined, an external memory engine, and a hash engine.

16 Claims, 7 Drawing Sheets



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Previous patent

US005404550A

United States Patent [19]

Horst

[11] Patent Number: 5,404,550

[45] Date of Patent: Apr. 4, 1995

[54] METHOD AND APPARATUS FOR EXECUTING TASKS BY FOLLOWING A LINKED LIST OF MEMORY PACKETS

[75] Inventor: Robert W. Horst, Champaign, Ill.

[73] Assignee: Tandem Computers Incorporated, Cupertino, Calif.

[21] Appl. No.: 736,594

[22] Filed: Jul. 18, 1991

[51] Int. Cl.[6] G06F 3/00

[52] U.S. Cl. 395/800; 364/232.22;232.91; 364/DIG. 1

[58] Field of Search ..... 395/800, 400, 275, 325, 375/650, 375; 364/200, DIG. 1, DIG. 2, 232.22, 232.91

[56] References Cited

U.S. PATENT DOCUMENTS

3,962,706	6/1976	Dennis et al.	395/650
4,149,240	4/1979	Mizuno et al.	395/800
4,153,932	5/1979	Dennis et al.	395/800
4,837,676	6/1989	Rowson	395/325
4,891,124	1/1990	Davidson et al.	395/800
4,972,315	11/1990	Yamasaki et al.	395/400
5,021,947	6/1991	Campell et al.	395/700
5,043,890	8/1991	Yoshida	395/375
5,083,919	8/1992	Yoshida et al.	395/800
5,117,489	5/1992	Kenort et al.	395/375
5,179,665	1/1993	Nofzi	395/425

OTHER PUBLICATIONS

Jeh et al. "WSI Architecture for L-U Decomposition: A Radar Array Processor", IEEE Feb. 1990, pp. 102–108.

Ramaswamy "A Methodology for Wafer Scale Integration of Linear Pipelined", IEEE Feb. 1990, pp. 220–228.

Robert Whiting Horst. "Task Flow: A Novel Approach to Fine-Grain, Wafer-Scale Parallel Computing", Thesis Submitted to University of Illinois at Urbana-Champaign, Apr. 1991.

Robert W. Horst, "A Linear-Array WSI Architecture for Improved Yield and Performance", proc. Int'l Conf. on Wafer Scale Int. Jan., 1990.

Srini, Vason P., "An Architectural Comparison of Dataflow Systems", IEEE, Mar. 1986, pp. 68–88.

Arvind and Culler, David E., "Dataflow Architectures", Ann. Rev. Comput. Sci., 1986, 1:225–53.

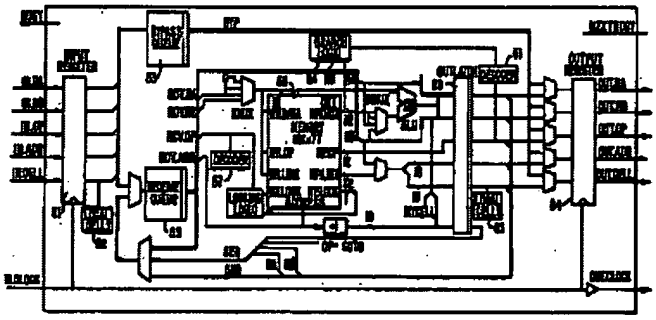
Nikhil, R. S. and Arvind, "Can dataflow subsume von Neumann Computing?", MIT Lab. for Comp. Science, 1989, pp. 262–272.

Papadopoulos & Culler, "Monsoon an Explicit Token-Store Architecture", IEEE, 1990, pp. 82–91.

Borker, Shekhar, et al., "Supporting Systolic and Memory Communication in iWarp", 17th Int'l Symp. on Computer Architecture, May 1990, pp. 1–40.

Primary Examiner—Alyssa H. Bowler
Assistant Examiner—D. Nguyen
Attorney, Agent, or Firm—Townsend and Townsend Khourie and Crew

[57] ABSTRACT

A computer architecture has a plurality of processing cells interconnected to perform programming tasks. Each cell contains both memory and processing elements. Memory packets contain an instruction, a data element, and a pointer to another memory packet. Tasks are executed by following a linked list of memory packets. Transmission packets communicate instructions and register values along the linked list. A plurality of computer processes may be executed simultaneously.

35 Claims, 13 Drawing Sheets